Super resolution implementation on FPGA

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STAGE 1

```
for i = 1 : conv1_filters
    conv1_data(:,:,i) = imfilter(im_b, weights_conv1(:,:,i), 'same',
'replicate');
    conv1_data(:,:,i) = max(conv1_data(:,:,i) + biases_conv1(i), 0);
end
```

STAGE 2

```
for i = 1 : conv2_filters
    for j = 1 : conv1_filters
        conv2_data(:,:,i) = conv2_data(:,:,i) + weights_conv2(j,:,i) *
conv1_data(:,:,j);
    end
    conv2_data(:,:,i) = max(conv2_data(:,:,i) + biases_conv2(i), 0);
end
```

STAGE 3

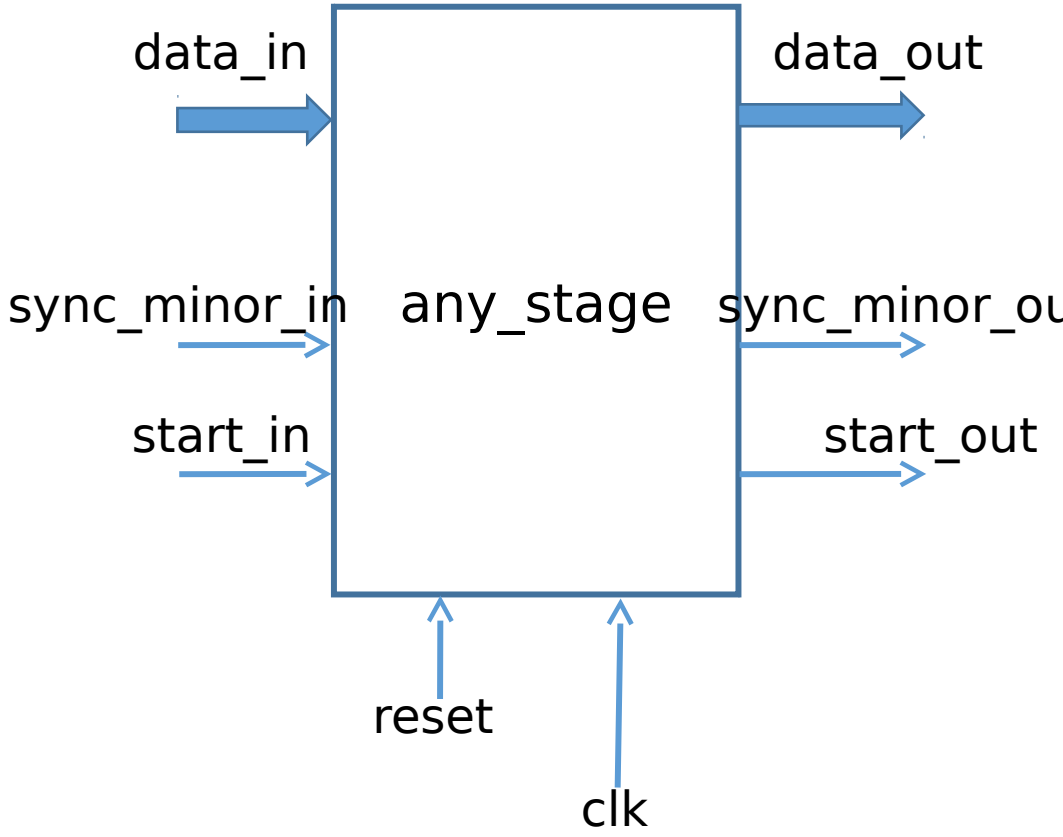
```
for i = 1 : conv2_filters
    conv3_subfilter = reshape(weights_conv3(i,:), conv3_patchsize,
conv3_patchsize);
    conv3_data(:,:) = conv3_data(:,:) + imfilter(conv2_data(:,:,i),
conv3_subfilter, 'same', 'replicate');
end
```

Synchronization scheme

Each stage or sub-stage in the pipeline consistently has the following control signals

1. reset : in
2. clk : in
3. sync_minor_in : in
4. start_in : in
5. sync_minor_out : out
6. start_out : out

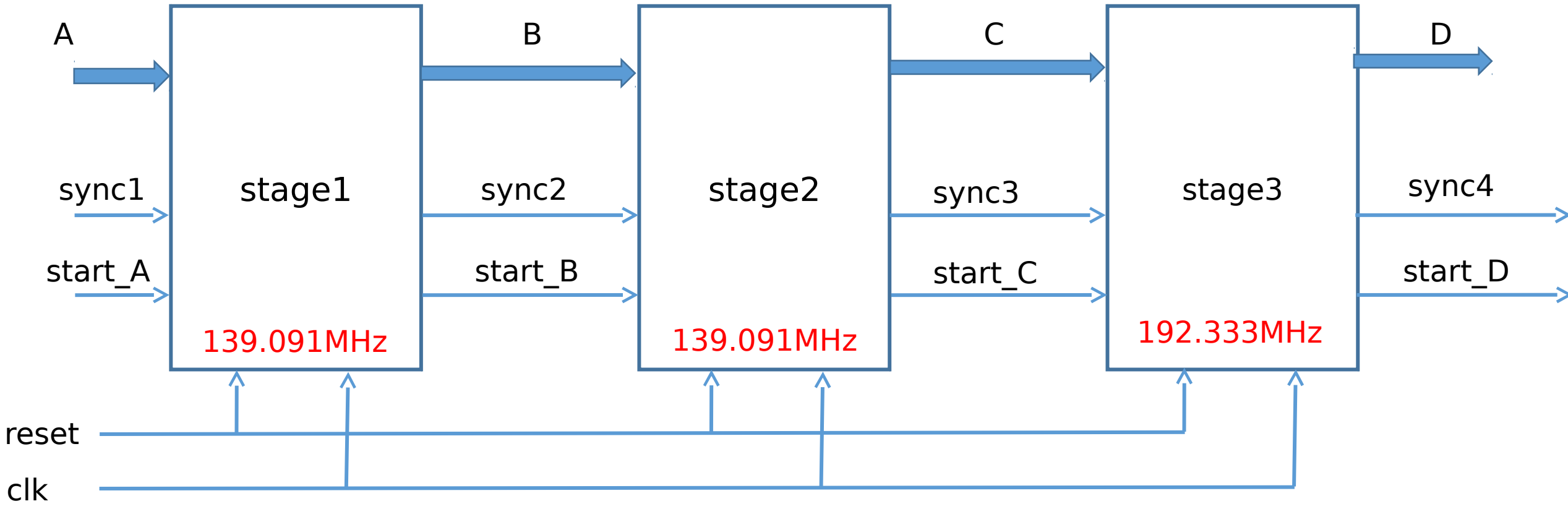
Specifications of these signals are given in the following slides



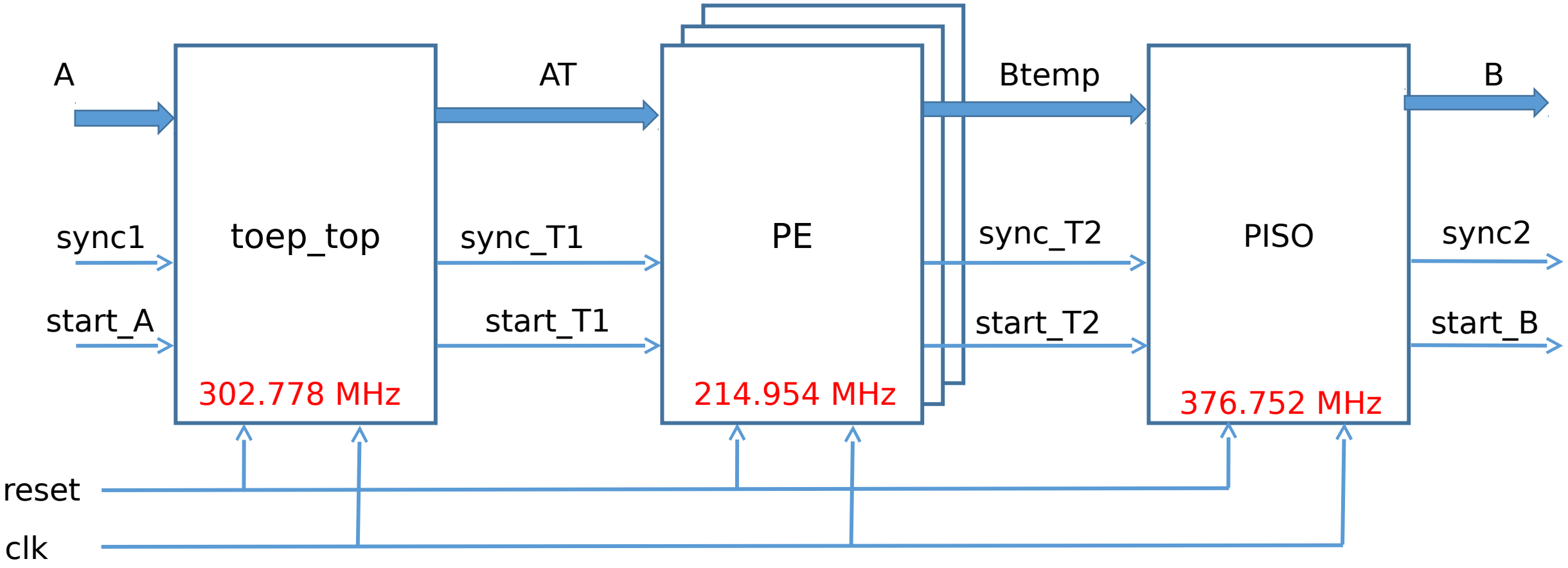
Signals start_in, start_out

- These signals have one pulse for each image frame, coinciding with the first sync_minor pulse of the frame.
- The ON duration of these pulses coincides with one clk period, indicating start of the ‘frame’.
- start_in (start_out) = 1 indicates availability of the first value of data_in (data_out) for the current frame.
- start_out may be delayed with respect to start_in by an integral number of minor cycles plus an integral number of clk periods. Each of these two numbers may be zero or more .

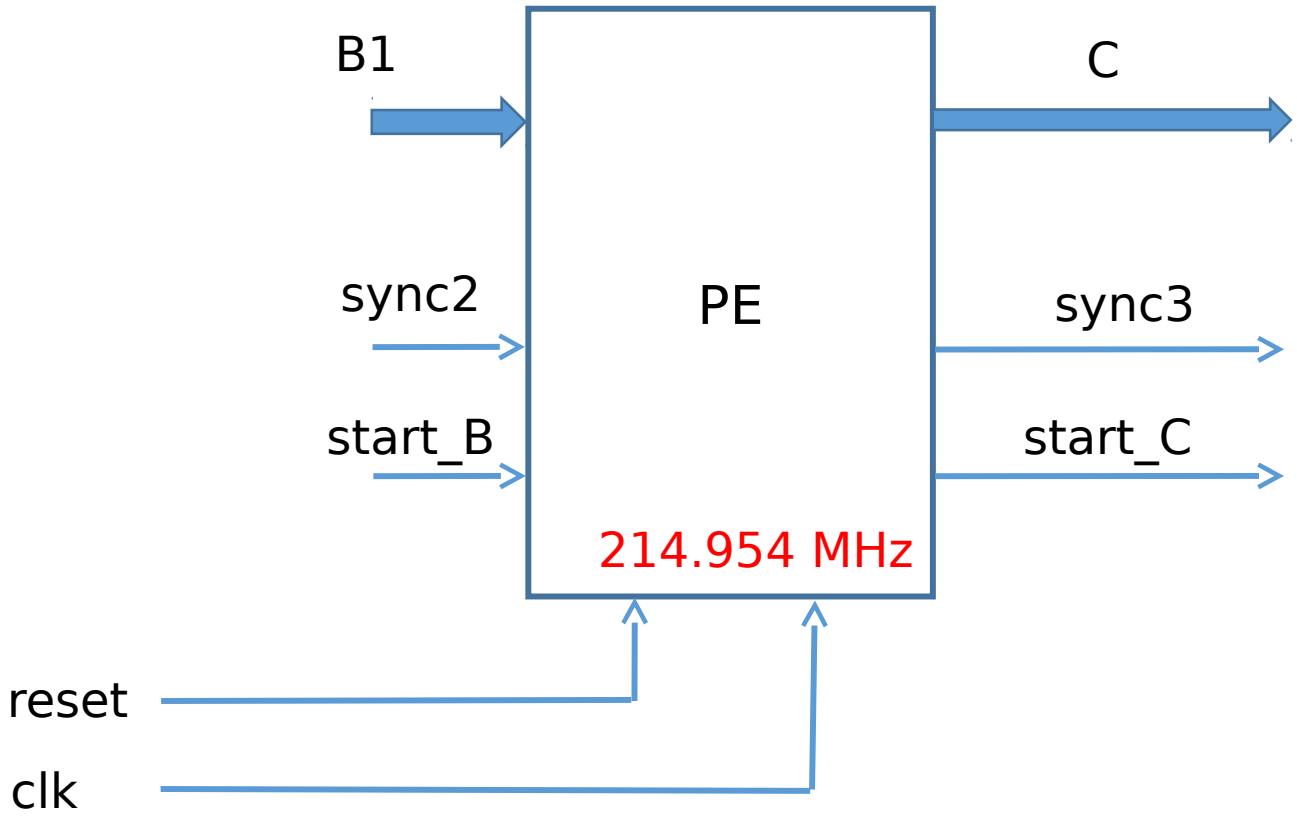
TOP Level Super_Resolution block diagram



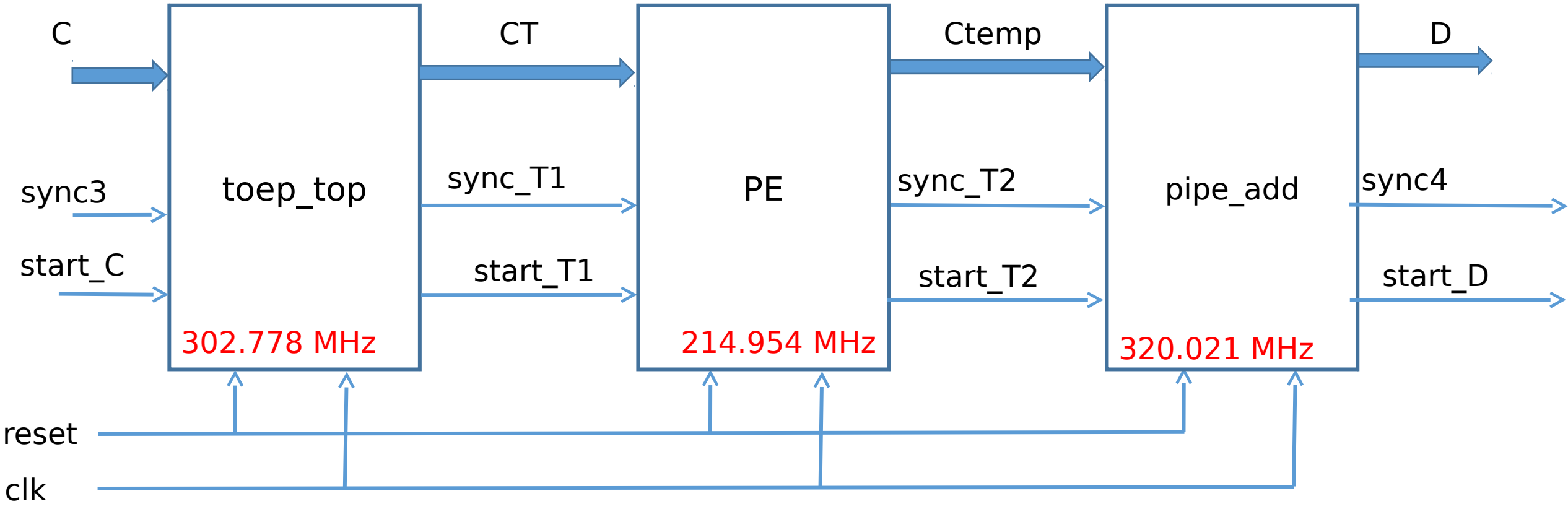
Stage1 block diagram



Stage2 block diagram

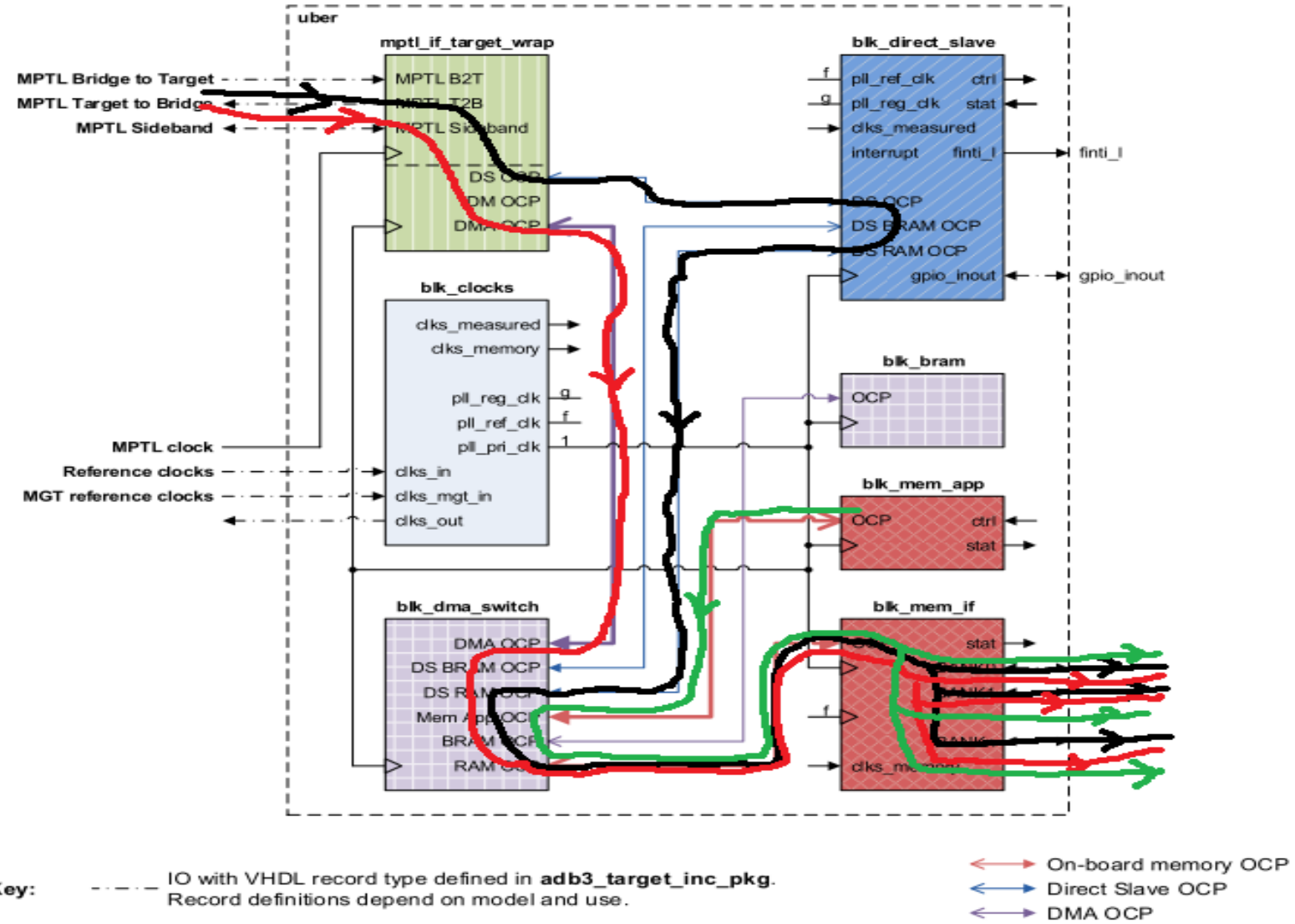


Stage3 block diagram



DDR3 INTERFACE

Data flow path from host to DDR3 SDRAM



UBER Design

- In the Uber design, there are two things that can access the DDR3 SDRAM on the card:
  - The host, via the MPTL interface. The host can access any of the 4 banks by using the appropriate OCP address.
  - The RAM “blk_mem_app", since it is multiplexed via the OCP interface to the module accessing 4 banks of DDR3.

IN-built protocols in UBER Design

- OCP Protocol
- MIG Protocol
  - Everything is OCP protocol *except* that inside "blk_mem_if", OCP signals are converted to MIG native interface protocol (app_* signals). The black is when the CPU accesses RAM. The red is when a DMA engine accesses RAM
  - To access the DDR3 SDRAM from an algorithm inside the FPGA, changes have been done in "blk_mem_app" (but we have used OCP protocol, not MIG native interface protocol). This data path is marked in green.
  - If we really have to use MIG native interface protocol, then we will have to make bigger changes to the structure of the Uber design. For example, we have to find a way to multiplex two MIG native interface channels together so that both channels can access a bank of DDR3 SDRAM.
  - Therefore, OCP protocol has been chosen that will govern the access of DDR3 to the super_resolution module via BRAM. The blk_dma_switch module is a module that multiplexes two or more OCP channels onto one OCP channel.

DATA-PATHS IN UBER

- Host Direct Slave (MPTL interface) <--OCP--> DDR3 SDRAM bank 0 (blk_mem_if)
- Host Direct Slave (MPTL interface) <--OCP--> DDR3 SDRAM bank 1 (blk_mem_if)
- Host Direct Slave (MPTL interface) <--OCP--> DDR3 SDRAM bank 2 (blk_mem_if)
- Host Direct Slave (MPTL interface) <--OCP--> DDR3 SDRAM bank 3 (blk_mem_if)

- our convolver (blk_mem_app) <--OCP--> DDR3 SDRAM bank 0 (blk_mem_if)
- our convolver (blk_mem_app) <--OCP--> DDR3 SDRAM bank 1 (blk_mem_if)
- our convolver (blk_mem_app) <--OCP--> DDR3 SDRAM bank 2 (blk_mem_if)
- our convolver (blk_mem_app) <--OCP--> DDR3 SDRAM bank 3 (blk_mem_if)

OCP Burst Write

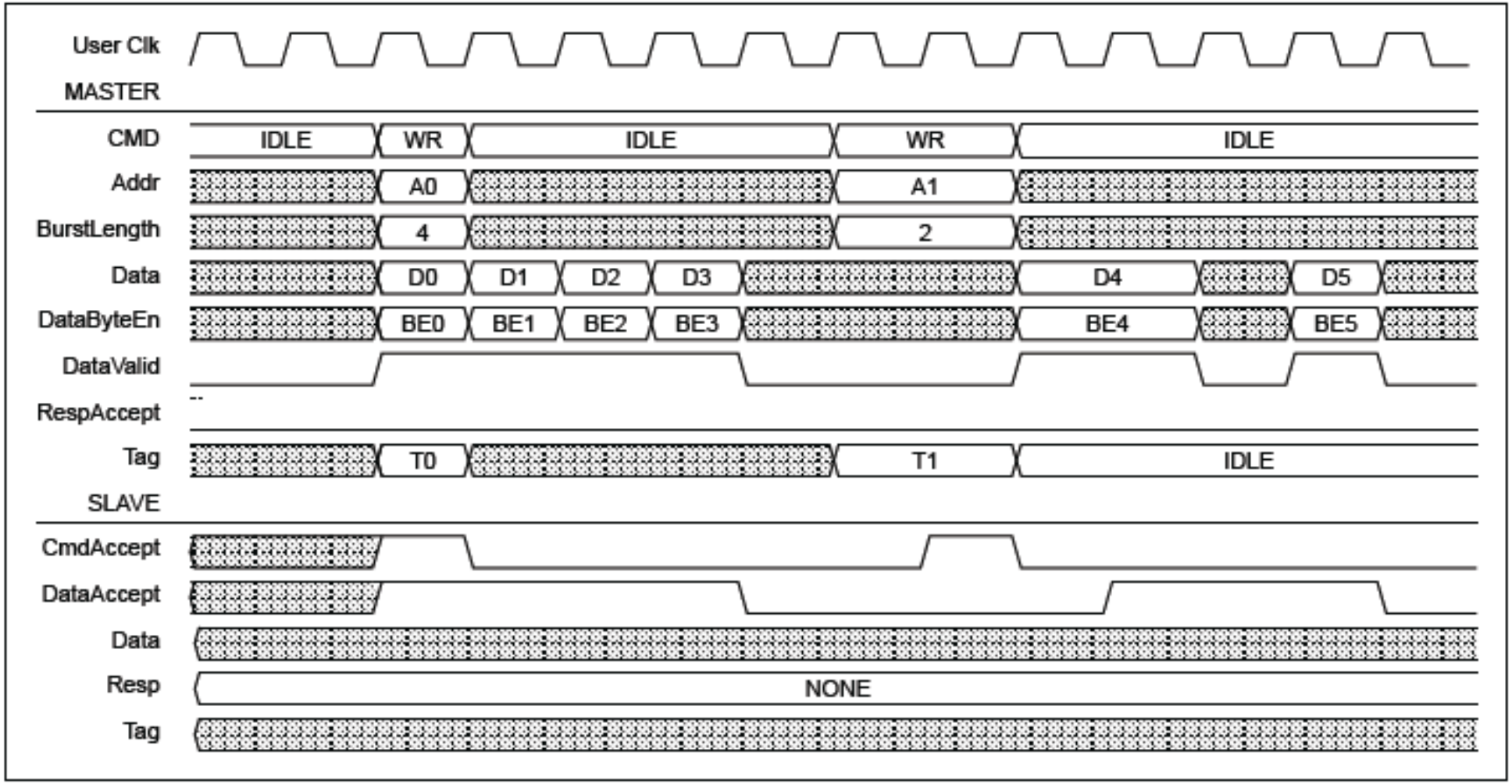


Figure 3 : Burst Write

OCP Burst Read

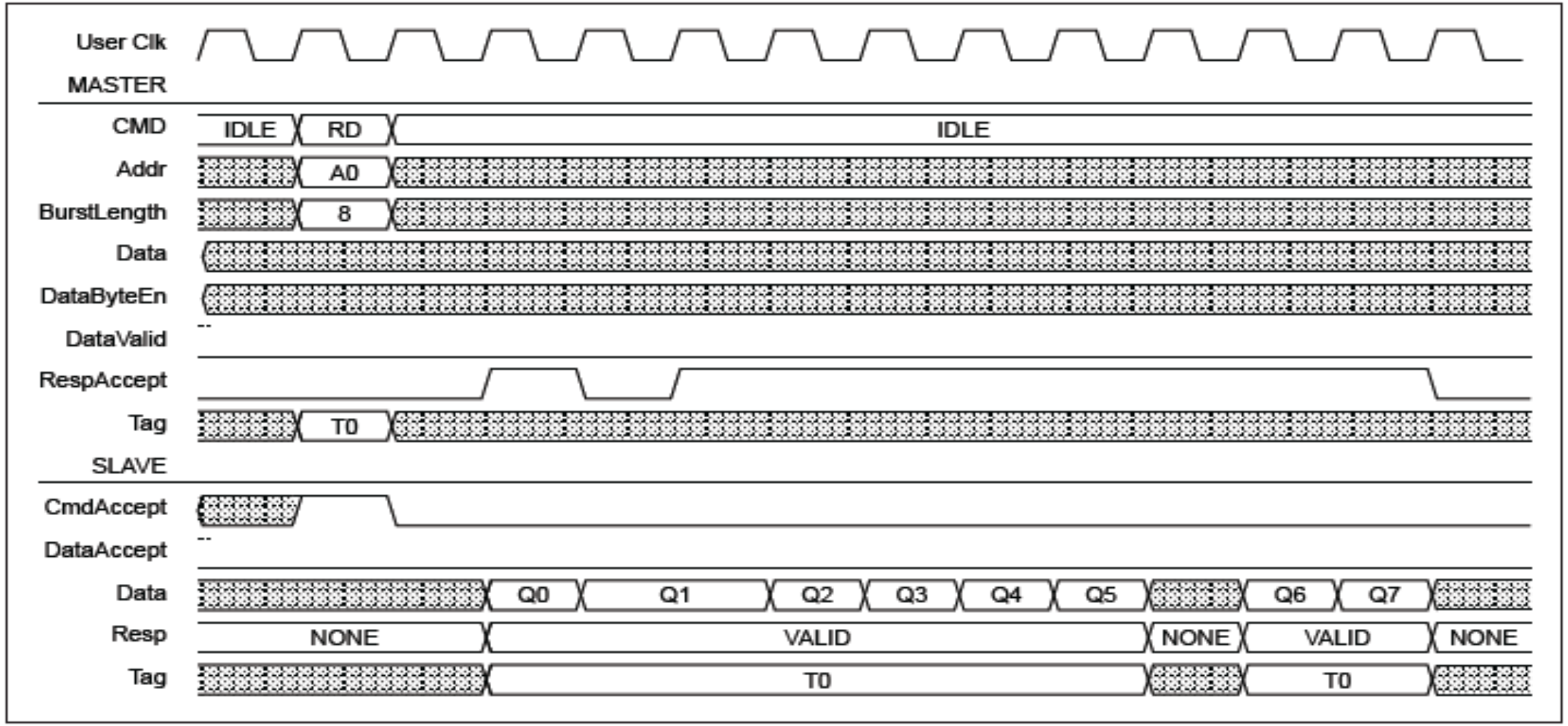
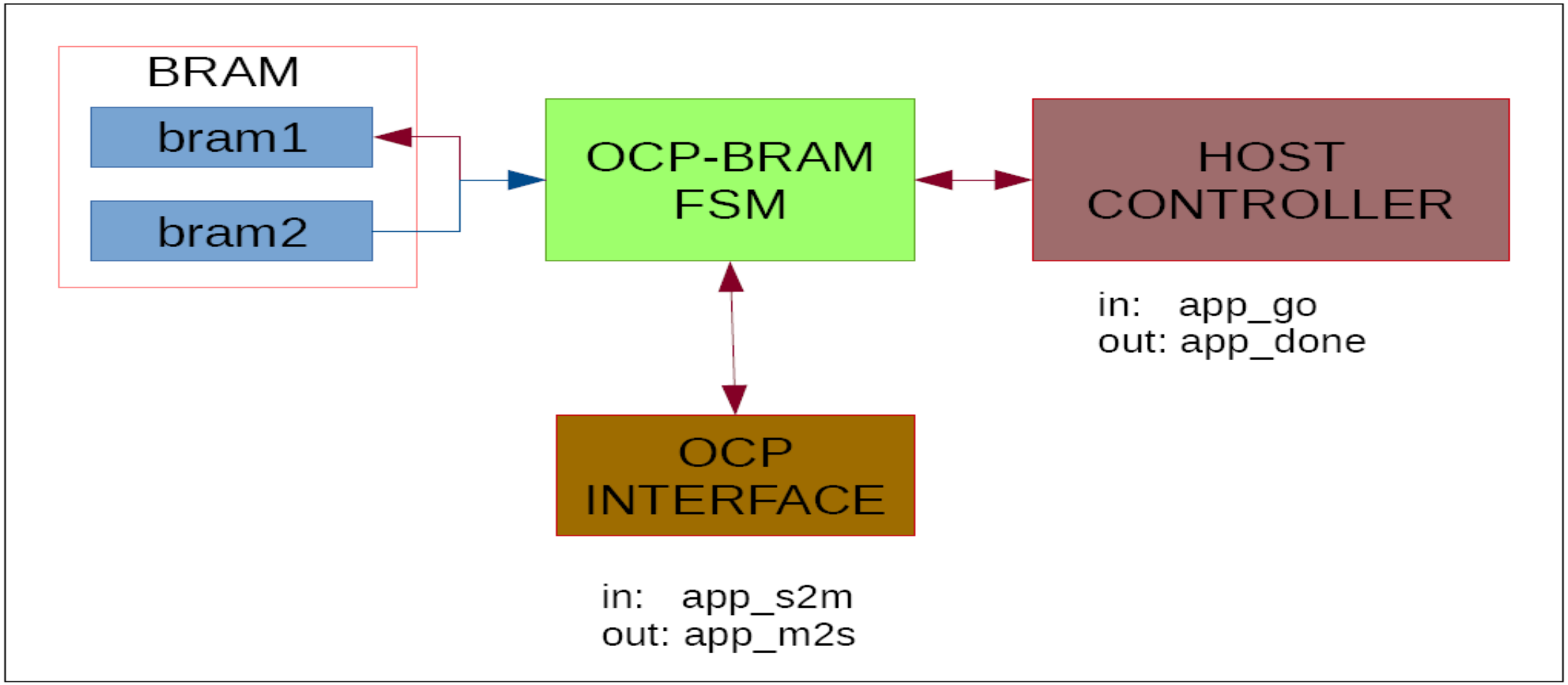


Figure 4 : Burst Read

Top level block diagram of blk_mem_app



DEVICE UTILIZATION SUMMARY

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	48	595200	0%
Number of Slice LUTs	64	297600	0%
Number of fully used LUT-FF pairs	32	80	40%
Number of bonded IOBs	42	600	7%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	2	2016	0%

PE

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	73	595200	0%
Number of Slice LUTs	300	297600	0%
Number of fully used LUT-FF pairs	53	320	16%
Number of bonded IOBs	600	600	100%
Number of BUFG/BUFGCTRLs	1	32	3%

PIPE_ADDER

DEVICE UTILIZATION SUMMARY (Contd..)

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	3772	595200	0%
Number of Slice LUTs	11044	297600	3%
Number of fully used LUT-FF pairs	3752	11064	33%
Number of bonded IOBs	42	600	7%
Number of Block RAM/FIFO	18	1064	1%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	128	2016	6%

Parallel to Serial Converter (PISO)

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	48	595200	0%
Number of Slice LUTs	64	297600	0%
Number of fully used LUT-FF pairs	32	80	40%
Number of bonded IOBs	42	600	7%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	2	2016	0%

TOEPLITZ

DEVICE UTILIZATION SUMMARY (Contd..)

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1837	595200	0%
Number of Slice LUTs	3256	297600	1%
Number of fully used LUT-FF pairs	1410	3683	38%
Number of bonded IOBs	600	600	100%
Number of Block RAM/FIFO	32	1064	3%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	64	2016	3%

STAGE 1

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1758	595200	0%
Number of Slice LUTs	4984	297600	1%
Number of fully used LUT-FF pairs	1748	4994	35%
Number of bonded IOBs	662	600	110%
Number of Block RAM/FIFO	8	1064	0%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	64	2016	3%

STAGE 2

DEVICE UTILIZATION SUMMARY (Contd..)

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	183	595200	0%
Number of Slice LUTs	510	297600	0%
Number of fully used LUT-FF pairs	180	513	35%
Number of bonded IOBs	42	600	7%
Number of Block RAM/FIFO	2	1064	0%
Number of BUFG/BUFGCTRLs	1	32	3%

STAGE 3

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	29472	595200	4%
Number of Slice LUTs	77012	297600	25%
Number of fully used LUT-FF pairs	26684	79800	33%
Number of bonded IOBs	162	600	27%
Number of Block RAM/FIFO	232	1064	21%
Number of BUFG/BUFGCTRLs	2	32	6%
Number of DSP48E1s	1024	2016	50%

SUPER_RESOLUTION